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EXAMINER

FLANDERS, ANDREW C

ART UNIT PAPER NUMBER

2644

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/922,816

Applicant(s)

BLESSER, BARRY A.

Examiner

Andrew C. Flanders

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 May 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-59 is/are pending in the application.
- 4a) Of the above claim(s) 3-12, 21-41, 44-52, 55 and 56 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 13-20, 42, 43, 53, 54 and 57-59 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

During a telephone conversation with Bruce Jobse on 07 June 2005 an election was made without traverse to prosecute the invention of the reverberation system of Fig. 1, claims 1, 2, 13 – 20, 42 – 43, 53 – 54 and 57 - 59. Affirmation of this election must be made by applicant in replying to this Office action. Claims 3 – 12, 21 – 41, 44 – 52 and 55 - 56 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Objections

Claim 1 objected to because of the following informalities: Claim 1 states “a plurality of gain minimum at the same frequencies”. It is unclear to the examiner as to what the same frequencies are. It appears as though the line should read “a plurality of gain minimum at the same frequencies as a plurality of delay maximum so that the decay rate...”. For the purpose of expediting prosecution the claim will be understood in this manner. Appropriate correction is required.

Claim2 objected to because of the following informalities: claim 2 recites “the second module and third multipliers operatively coupled to form an signal processing circuit” which should apparently read “the second module and third multipliers operatively coupled to form a signal processing circuit” Appropriate correction is required.

Claim Rejections - 35 USC § 101

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35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 42, 43 and 57 - 59 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 42 and 43 recite a set of logic steps within a signal bearing medium which require a computer to function. Claims 42 and 43 do not contain any pre or post processing limitations, they merely manipulate an abstract idea. For further information see MPEP section 2106 regarding computer related inventions.

Claims 57 – 59 recite program code for carrying out a set of steps on a computer. Claims 57 – 59 do not contain any pre or post processing limitations, they merely manipulate an abstract idea. Even though the claim does state the limitation of being useful for generating data representing a processed audio signal, it is still non statutory. Even though the program is capable of producing an output it doesn't necessarily always do that. For further information see MPEP section 2106 regarding computer related inventions.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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Claim 20 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 20 recites the limitation "a second delay module, for delaying the signal by a first delay value." It is unclear whether the second delay module or the first delay module or the combination creates the first delay value. Appropriate correction is required. For the purpose of expediting prosecution the first delay module will be understood to create the first delay value.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, 13 – 20, 42, 43, 53, 54 and 57 – 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rao (U.S. Patent 6,665,409).

Regarding **Claim 1**, Rao discloses:

A processing system capable of electronically generating reverberation signals having a decay rate (abstract), the system comprising:

(A) a notchpass filter for receiving a signal and generating an output signal (Fig. 8B), comprising:

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a first module for delaying the signal by a first delay value (Fig. 8B, the delay size block);

a first multiplier for scaling the signal according to a first gain (i.e. G1 of Fig. 8B and col. 10 lines 48 – 58);

a second multiplier for scaling the signal according to a second gain (i.e. G2 of Fig. 8B and col. 10 lines 48 – 58);

wherein the first module and first and second multipliers are operatively coupled to form a first signal processing circuit path (i.e. G1, G2 and the delay size block are all coupled according to the lines drawn within Fig. 8B);

the notchpass filter having a comb filter-like amplitude (i.e. each comb filter reproduces the input with a periodic delay and decaying amplitude; col. 10 lines 42 – 67);

(B) an energy transmission network for receiving the output signal from the notchpass filter (i.e. Fig. 8C and Fig. 8A), the energy transmission network comprising:

a second module for delaying the signal by a second delay value (i.e. Fig. 8C the delay size block);

a third multiplier for scaling the signal according to a third gain (i.e. Fig. 8C G1);

wherein the second module and third multipliers are operatively coupled to form a second signal processing circuit path that both delays and scales the received signal (i.e. G1 and the delay size block are all coupled according to the lines drawn within Fig. 8B);

the values of the first and second gain have a defined relationship with the first and second delay values and the third gain (i.e. G1 and G2 are derived automatically and the delays are set to avoid echoes; see col. 10 lines 47 – 67 and col. 11 lines 1 – 18).

Rao does not disclose a notchpass filter with delay output response characterized by a plurality of delay maximum at certain frequencies and a plurality of gain minimum at said certain frequencies or the combined notchpass filter and energy transmitting network have an amplitude response characterized by a plurality of gain minimum at the same frequencies and a plurality of delay maximum at the same frequencies so that the decay rate is substantially identical at all frequencies.

However, choosing a notchpass filter with a plurality of delay maximums at the same location as the gain minimums is a design choice by applicant. Notch pass filters can be adjusted to add more or less notches or shift the locations of the notches among the frequency spectrum. Aligning them with the delay peaks would have been obvious (i.e. notchpass filter with delay output response characterized by a plurality of delay maximum at certain frequencies and a plurality of gain minimum at said certain frequencies).

Furthermore, by adding this design choice the filter inherently will have the property of the decay rate being substantially identical at all frequencies.

Regarding **Claim 2**, Rao discloses:

A method for electronically generating reverberation signals having a decay rate (abstract), the method comprising:

(A) providing a notchpass filter in combination with an energy transmission network (Fig. 8A, the notchpass filter and all pass filter system), where the notchpass filter comprises:

a first module for delaying the signal by a first delay value (Fig. 8B, the delay size block);

a first multiplier for scaling the signal according to a first gain (i.e. G1 of Fig. 8B and col. 10 lines 48 – 58);

a second multiplier for scaling the signal according to a second gain (i.e. G2 of Fig. 8B and col. 10 lines 48 – 58);

the first module and first and second multipliers operatively coupled to form an signal processing circuit path(i.e. G1, G2 and the delay size block are all coupled according to the lines drawn within Fig. 8B);

the notchpass filter having a comb filter-like amplitude (i.e. each comb filter reproduces the input with a periodic delay and decaying amplitude; col. 10 lines 42 – 67);

the energy transmitting network comprising:

a second module for delaying the signal by a second delay value (i.e. Fig. 8C the delay size block);

a third multiplier for scaling the signal according to a third gain (i.e. Fig. 8C G1);

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the second module and third multipliers operatively coupled to form a signal processing circuit path that both delays and scales the received signal (i.e. G1 and the delay size block are all coupled according to the lines drawn within Fig. 8B);

(B) calculating modified first and second gain value from the first and second delay values and the first, second and third gain (i.e. G1 and G2 are derived automatically and the delays are set to avoid echoes; see col. 10 lines 47 – 67 and col. 11 lines 1 – 18); and

(C) applying the modified first and second gain value to the first and second multipliers, respectively (i.e. the coefficients for G1 and G2 are set and the all pass filters are used to decorrelate the different channel outputs from each other, the delay sizes are fixed and the coefficients are set for stability depending on increasing or decreasing parameters; col. 11 lines 7 – 17).

Rao does not disclose a notchpass filter with delay output response characterized by a plurality of peak delay maximum at certain frequencies and decreased gain minimum at the same certain frequencies or the combined notchpass filter and energy storing network has an amplitude output response characterized by a plurality of gain minimum at the same certain frequencies and a plurality of delay maximum at the same certain frequencies so that the decay rate is substantially identical at all frequencies.

However, choosing a notchpass filter with a plurality of delay maximums at the same location as the gain minimums is a design choice by applicant. Notch pass filters can be adjusted to add more or less notches or shift the locations of

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the notches among the frequency spectrum. Aligning them with the delay peaks would have been obvious (i.e. notchpass filter with delay output response characterized by a plurality of delay maximum at certain frequencies and a plurality of gain minimum at said certain frequencies).

Furthermore, by adding this design choice the filter inherently will have the property of the decay rate being substantially identical at all frequencies.

Regarding **Claim 13**, Rao discloses:

A signal processing system (abstract) comprising:

a first delay module for creating an output signal (Fig. 8B, the delay size block);

a first multiplier for scaling the output signal with a first gain (i.e. G1 of Fig. 8B and col. 10 lines 48 – 58);

a second multiplier for scaling the output signal, modified by the first gain with a second gain (i.e. G2 of Fig. 8B and col. 10 lines 48 – 58);

a filter formed from the first delay module, the first multiplier, and the second multiplier for creating a comb filter-like amplitude (i.e. a comb filter; col. 10 lines 42 – 67).

Rao does not disclose and delay output response characterized by a plurality of peak delay maximum at certain frequencies and decreased gain minimum at the same certain frequencies.

However, choosing a notchpass filter with a plurality of delay maximums at the same location as the gain minimums is a design choice by applicant. Notch pass filters can be adjusted to add more or less notches or shift the locations of the notches among the frequency spectrum. Aligning them with the delay peaks would have been obvious to one of ordinary skill in the art at the time of the invention (i.e. notchpass filter with delay output response characterized by a plurality of delay maximum at certain frequencies and a plurality of gain minimum at said certain frequencies).

Regarding **Claim 14**, in addition to the elements stated above regarding claim 13, Rao further discloses:

The signal processing of claim 13 in serial combination with an energy transmission network for processing a signal (Fig. 8A, the notchpass filters and all pass filters); the energy transmission network comprising:

a second delay module capable of creating a second output (i.e. Fig. 8C the delay size block);

a third multiplier for scaling the second output by a third gain (i.e. Fig. 8C G1);

where the second delay module and the third multiplier are operatively coupled to form a third output signal (i.e. G1 and the delay size block are all coupled according to the lines drawn within Fig. 8B).

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Regarding **Claim 15**, in addition to the elements stated above regarding claim 14, Rao further discloses:

wherein a portion of the second output signal is processed and filtered (i.e. the output of the delay module is part of the all pass filter and thus is inherently part of a filtering process; Fig. 8C).

Regarding **Claim 16**, in addition to the elements stated above regarding claim 15, Rao further discloses:

A plurality of the processing systems of claim 15 coupled in parallel with a source signal (i.e. the all pass filters coupled in parallel in Fig. 8A).

Regarding **Claim 17**, in addition to the elements stated above regarding claim 15, Rao further discloses:

A plurality of the processing systems in claim 15 coupled in series with a source signal (i.e. the main all pass filter is coupled in series with the other all pass filters; Fig. 8C).

Regarding **Claim 18**, in addition to the elements stated above regarding claim 14, Rao further discloses:

The processing system of claim 14 in combination with one or more filters with frequency responses having one of increased and decreased gain at certain frequencies (i.e. the notchpass filters of fig 8A have the characteristic of increased and decreased gain at certain frequencies).

Regarding **Claim 19**, in addition to the elements stated above regarding claim 14, Rao further discloses:

Wherein a first filter is coupled in series with the second delay module (i.e. the comb filters are in series with the all pass filters which contain the second delay block; fig. 8A);

and a second filter is combined with one of the first and second multipliers (i.e. the all pass filter is combined with the comb filters which contain the first and second multipliers).

Regarding **Claim 20**, in addition to the elements stated above regarding claim 13, Rao further discloses:

a second delay module, in series with the first delay module, for delaying the signal by the first delay value (i.e. the delay block in the comb filter is in series with the delay block in the all pass filter; fig 8A, B and C);

the first multiplier configured in parallel with the first module in a feedback circuit path (i.e. G1 is in parallel with the first module and G2 is in parallel with the second; Figs 8B and 8C).

Regarding **Claims 42, 43, 53, 54, and 57 - 59**, they are interpreted and thus rejected for the same reasons as set forth above in claim 1.

Conclusion

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The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hewitt (U.S. Patent 5,896,291) and Kowaki (U.S. Patent 5,247,474).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Flanders whose telephone number is (571) 272-7516. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on (571) 272-7848. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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